

The New Paradigm Shift for High-Performance Computing

4th European LS-DYNA Conference
May 23rd, 2003
Ulm, Germany

Dr. Herbert Cornelius
Intel EMEA



Agenda

HPC Industry and Market Trends

Driving the Change in HPC

HPC Building Blocks

HPC Solutions

Software Toolset



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2



CAE Challenges

Shorten Design and Development Time

- Shorten time-to-market
- Reduce expensive and time consuming mechanical tests
- Reduce material (costs, weight, new)
- Optimize specific features, e.g.
 - Statics
 - Dynamics
 - Kinematics
 - Aero & Hydro Dynamics
 - Safety
 - Temperature

Solution: High-Performance Computing (HPC)

Numerical analysis and simulations on high-performance systems

- Increase Capacity
- Increase Capability
- Better Flexibility
- More Cost Effective
- Leverage Volume Economics

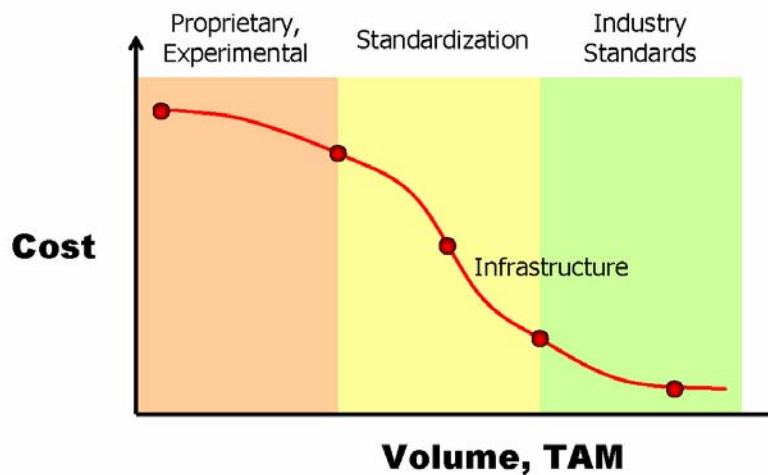


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The Standardization Curve



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Some HPC History



1960s 1970s 1980s 1990s 2000s

HPC Systems	1970s	1980s	1990s	2000s
Processor	proprietary	proprietary	COTS	COTS
Memory	proprietary	proprietary	COTS	COTS
Motherboard	proprietary	proprietary	proprietary	COTS
Interconnect	proprietary	proprietary	proprietary	COTS
OS, SW Tools	proprietary	proprietary	proprietary	COTS

COTS: Commercial off the Shelf (industry standard)



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5

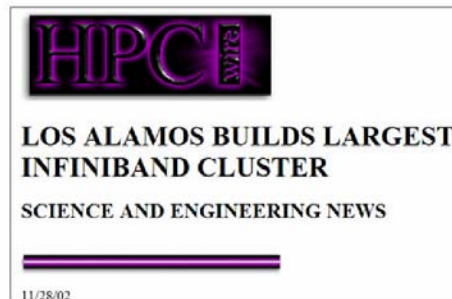


The Growing Popularity of (SMP-)Cluster Computing



2,304 Intel® Xeon™ 2.4 GHz processors power this 5.69 TFlops supercomputer at Lawrence Livermore National Labs. It rates as the fifth fastest in the world.

The number of clusters in the TOP500 has grown to nearly 20 percent, with a total of 93 systems. 56 of them are Intel Architecture based.



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HPC is Changing

**Proprietary
Expensive**



**Industry Standards
Building Blocks for
Volume Economics**

Processor	→	Intel® Architecture
Architecture	→	Cluster of SMP nodes
OS	→	Linux*, Windows*
Parallel API	→	OpenMP*, MPI*
Performance	→	following Moore's Law
Costs	→	Affordable



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7



HPC Building Blocks

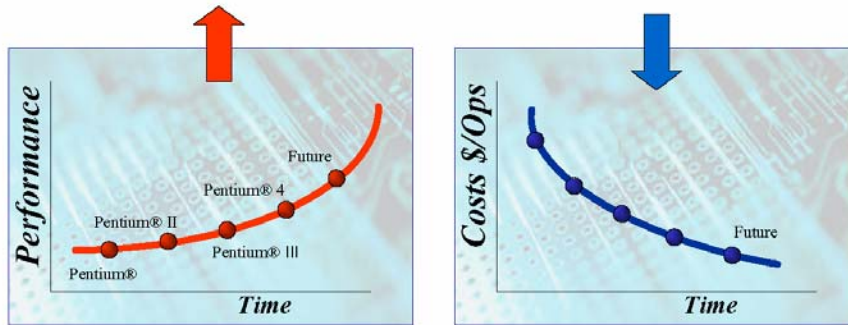


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8



Why Intel® Architecture is so attractive



We are at an "Inflection Point" and Paradigm Shift in HPC ... Clusters of SMP nodes

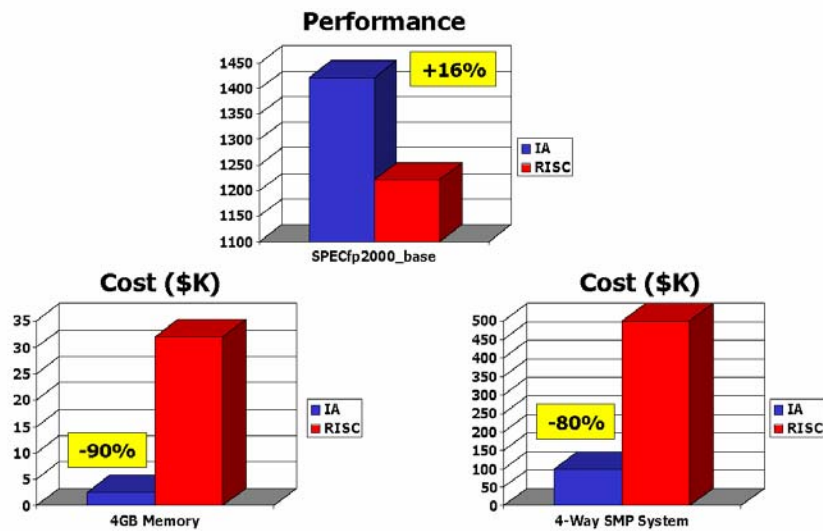


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10



Economy of Scale



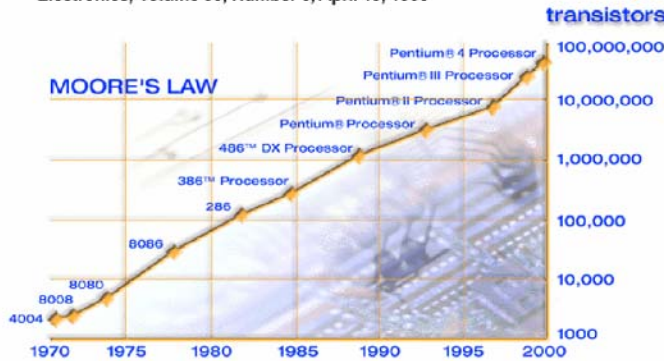
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11



Driving The Change in Computing Economics

Electronics, Volume 38, Number 8, April 19, 1965



**10GHz
1 Billion
Transistors
~2007 (est.)**

**Enabling
Peta-Flop
Computing**

www.intel.com/research/silicon



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12



Improving Performance

Intel Research & Development

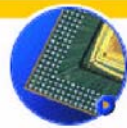
Pioneering Innovation Through Technology Leadership



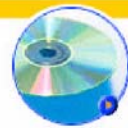
Silicon Technology & Manufacturing



Microarchitecture & Circuits



Computing Platforms



Software Technology



Communications & Networking

- Silicon Process
- Density
- Frequency
- Manufacturing

- Micro-Architecture
- Execution Units, Caches
- Threading
- Memory Subsystem
- I/O-Subsystem
- System Architecture

- Compilers
- Libraries
- Tools
- ISVs

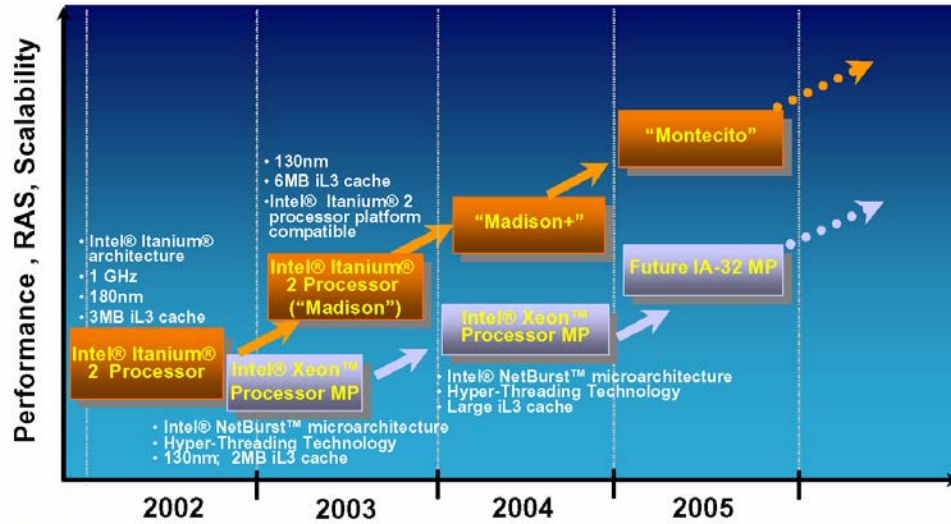


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13



Intel® Architecture MP Server Processor Roadmap



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14



Processor Architectures



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15



IA-32 Xeon™ Architecture



Xeon™ DP Server/Workstation Processor

3.06GHz Frequency
512KB integrated L2-Cache
533MHz Front-Side Bus
Dual-Channel DDR-266 Memory

Xeon™ MP Server Processor

2.0GHz Frequency
400MHz Front-Side Bus
2MB integrated L3-Cache
4+ way SMP Support



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intel.com

Are you ready?

The world's leading technology companies are united in their support for the Intel® Itanium® 2 processor, and are developing a range of enterprise solutions for your business.



High-performance technology for the most data-intensive, business-critical applications. Get ready to evaluate and deploy. The Intel® Itanium® processor family. The next enterprise architecture.



Yes. intel.

Providers developing Intel® Itanium® 2 processor based solutions:

Operating Systems:



Software Solutions:



Server / Workstation Hardware:



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Itanium® 2 Processor Performance

	Application Area	Benchmark	Results	Beats Best RISC By
Enterprise Computing	Enterprise Resource Planning	4P SAP SD ¹	600	IPF Alpha <i>Also #1 16P</i> 43%
	Supply Chain Demand Planning	4P SAP APO-DP ²	158K	IPF Alpha 15%
	On-line Transaction Processing	4P TPC-C (TPC-C) ³	87.7	IPF Alpha <i>Also #1 32P</i> 55%
	On-line Transaction Processing	4P TPC-C (\$/TPC-C) ³	\$5.03	IPF Alpha 47%
	Secure Transactions	4P SPECweb99_SSL ⁴	1888	IPF PA-RISC <i>Also #1 2P & 1P</i> 59%
Technical Computing	Matrix Multiplication	32P Linpack ⁵	101.7	IPF Power 4 7%
	Matrix Multiplication	1P Linpack ⁶	3534	IPF Power 4 22%
	Floating Point Computation	SPECfp_base2000 ⁷	1431	IPF Power 4 17%
	Memory Bandwidth	64P Stream Triad ⁸	125K	IPF 64P Sun 72P 146%

RISC comparisons based on publicly available RISC benchmark results as of 12/2002.

1 Source: www.sas.com. Itanium® 2 processor result on HP Server x8600 using 4 Itanium® 2 processors (10M) with 2GB L3 cache, 16GB memory, Windows Advanced Server LE 1.2, SAP net-6.5.2.52. Other Enterprise Edition 6000. Alpha result of 420 on HP AlphaServer C240 using 4 Alpha EV650 1000 42 GB memory.

2 Source: www.sap.com. Itanium® 2 processor result on HP Server x8600 using 4 Itanium® 2 processors (10M) with 2GB L3 cache, 16GB memory, Windows Advanced Server LE 1.2, SAP net-6.5.2.52. Other Enterprise Edition 6000. Alpha result of 420 on HP AlphaServer C240 using 4 Alpha EV650 1000 42 GB memory.

3 Source: www.tpc.org. Itanium® 2 processor result on HP Server x8600 using 4 Itanium® 2 processors (10M) with 2GB L3 cache, 16GB memory, HP-UX, Power 4 result of 284 on IBM eServer p690 using one Power4 1.0M.

4 Source: www.spec.org. Itanium® 2 processor result on HP Server x8600 using one Itanium® 2 processor (10M) with 2GB L3 cache, 16GB memory, HP-UX, Power 4 result of 284 on IBM eServer p690 using one Power4 1.0M.

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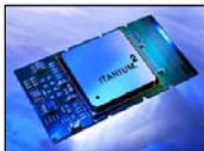
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Madison**



**codename

Next-Generation Itanium® Architecture Processor
130nm Process
410M Transistors
Up to 1.5GHz Frequency
6MB integrated L3-Cache
Pin-Compatible to Itanium® 2 Processor
Same Thermal Envelope
Low-Voltage Version (Deerfield)**

~1.3-1.5x faster than Itanium® 2

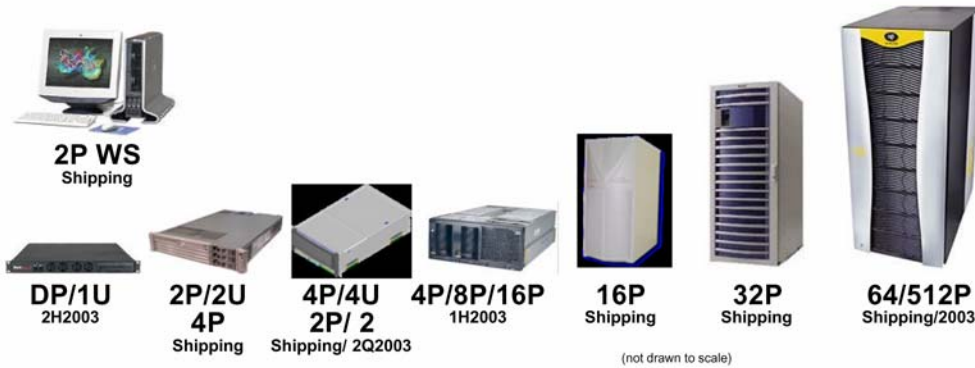


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Itanium® Architecture Systems

High-end Itanium® 2-based systems ...
 >2X more than Itanium !

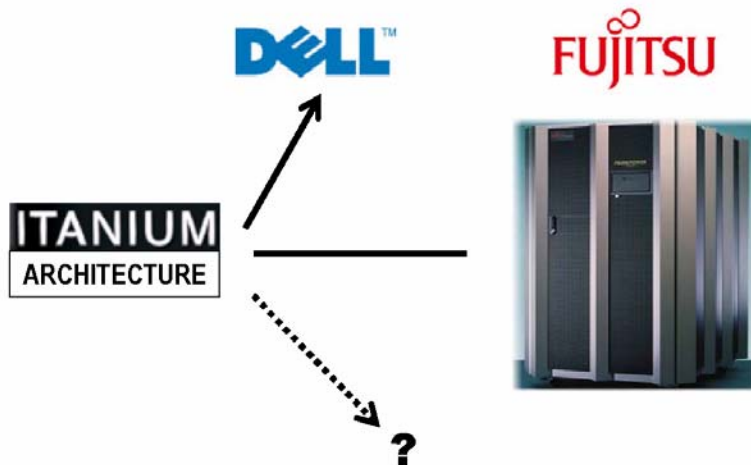


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20



The Move is on ...



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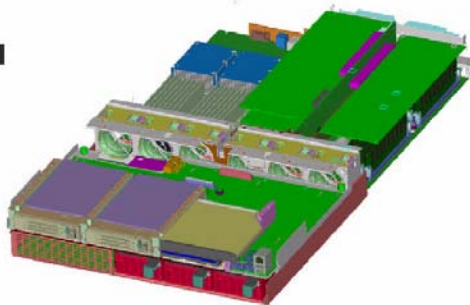
21



Itanium® 2 DP, 2u, E8870 System



**“Tiger-2” platform (SR870BH
Q2’03 target availability
Madison/Montecito ready
1-2 CPUs
8 DIMM slots (16GB)
3 PCI-X slots
2GbE on board
2H2003**

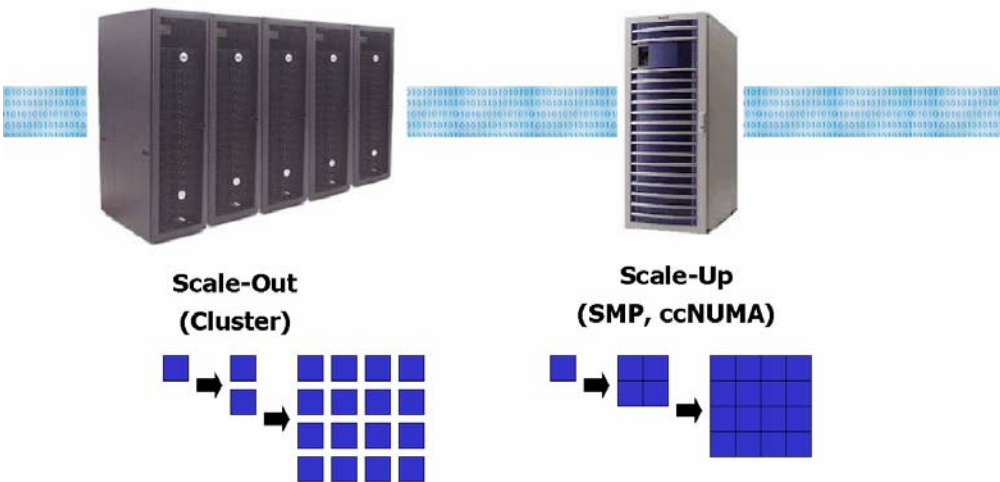


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22



Performance Scaling








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23



SMP Nodes






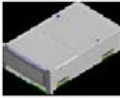

	⋮	
8u (1-8 CPUs)	Scalable	
4u (1-4 CPUs)	Expandable	
2u (1-2 CPUs)	Dense	
1u (1-2 CPUs)	Dense	
Blades	Ultra-Dense	



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24



	64-512P	<div style="background-color: #0056b3; color: white; padding: 5px; margin-bottom: 10px;">Do more, better and faster at lower costs.</div> <p>Increase Capacity and Capability</p> <p>Scaling Out and Scaling Up</p> <p>→ Scaling Right</p>	
	32P		
	16P		
	DP/1U		
	DP/2U		
		4P/4U	4P/8P/16P



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25

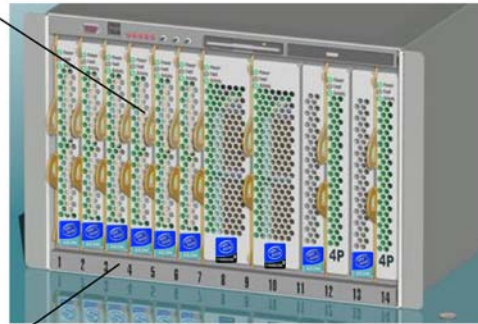


Blade Clusters – The Next Wave?

- Range of compute performance available
 - From initial release through first 9 months
- 2-way Intel® Xeon™ processor blade (1 slot)
- 4-way Xeon processor blade (2 slots)
- 2-way Itanium™ 2 processor blade (2 slots)
- Dual, redundant connectivity to backplane for LAN and storage networks
 - 1 Gb Ethernet
 - 2 Gb Fiber Channel

- 7U Chassis
 - 28" Depth
- 14 Compute Blade Slots
- Dual-Dual Star Backplane Topology
- Dual, Redundant Power Supply
- Dual, Redundant Blowers

Product concept:
compute blade and chassis



**Enabling
1 TFLOP in one Rack.**



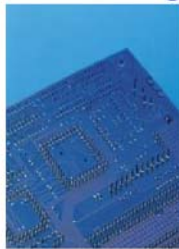
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26



Modular Scalable Computing

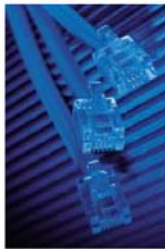
Processing



Memory



I/O



Storage



**Flexible and Balanced Solution
using Industry Standards**



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27



Interconnects

- 100Mbit/s, 1000Mbit/s Ethernet
- 10Gbit/s Ethernet
- GigaNet*
- SCI*
- Myrinet*
- QsNET*
- Infiniband*
- Crossbar (proprietary)
- [cc]NUMA (proprietary)



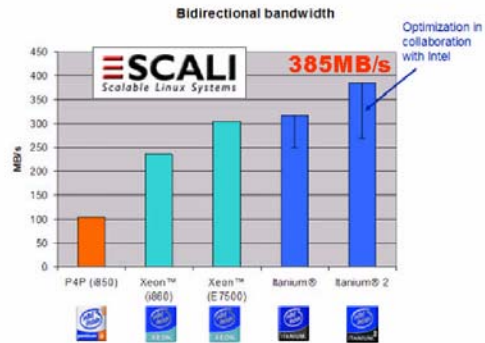
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28



Interconnects

QADRICS
1.2GB/s
multi-rail
on Itanium® 2



over 800 Mbytes/sec bandwidth and 8.7 microsecond latency



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29



Evolving Interconnects & Storage

INFINIBAND
FAST. RELIABLE.

Inter-Facility

Site to Site
Data Center
to Data Center

Inter-System

Rack to Rack

Intra-System

Blade to
Blade
within the
Rack

Intra-Board

Chip to Chip
Add-in Cards

Ethernet

InfiniBand*

PCI Express*

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30



Software Development Tools

SW Products

Compilers



Performance Libraries



VTune™ Performance Analyzer



Intel® Threading Tools



www.intel.com/products/software

Developer Services

www.intel.com/ids



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31



Summary

- **The Economics of High-Performance Computing have changed.**
- **High-Performance Computing solutions must track Moore's law to be viable.**
- **Intel is playing a key role in accelerating HPC solutions for science, engineering and business with open commercial off the shelf technology leadership.**



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32



Technology Leadership



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